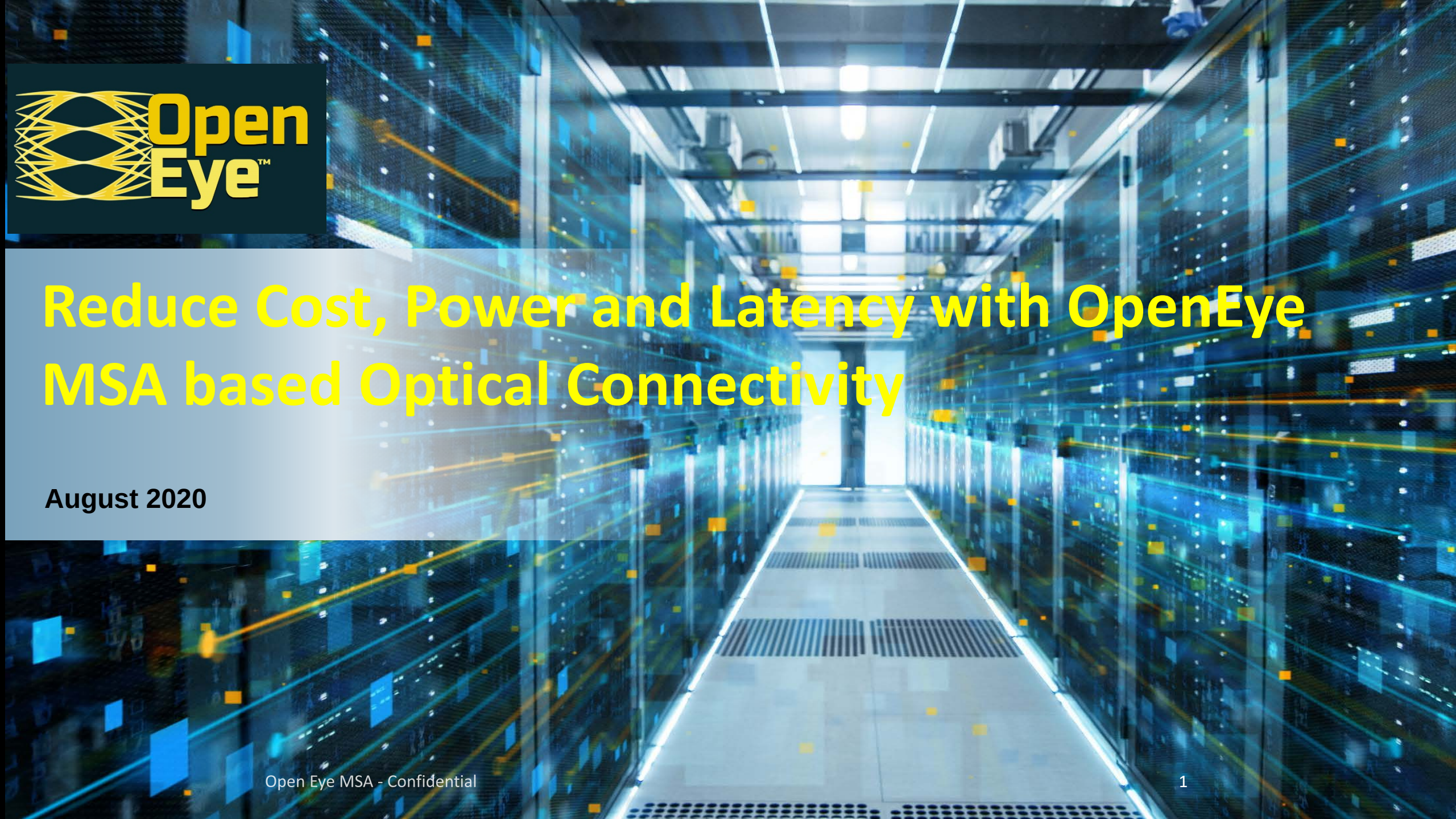


Reduce Cost, Power and Latency with OpenEye MSA based Optical Connectivity

August 2020

Open Eye MSA - Executive Summary

- **Problems to Solve:**
  - Support bandwidth growth while reducing cost and power per Gigabit
  - Assure multivendor interoperability
  - IEEE 400G Gbps Standards Practically Require use of DSP technologies for compliance

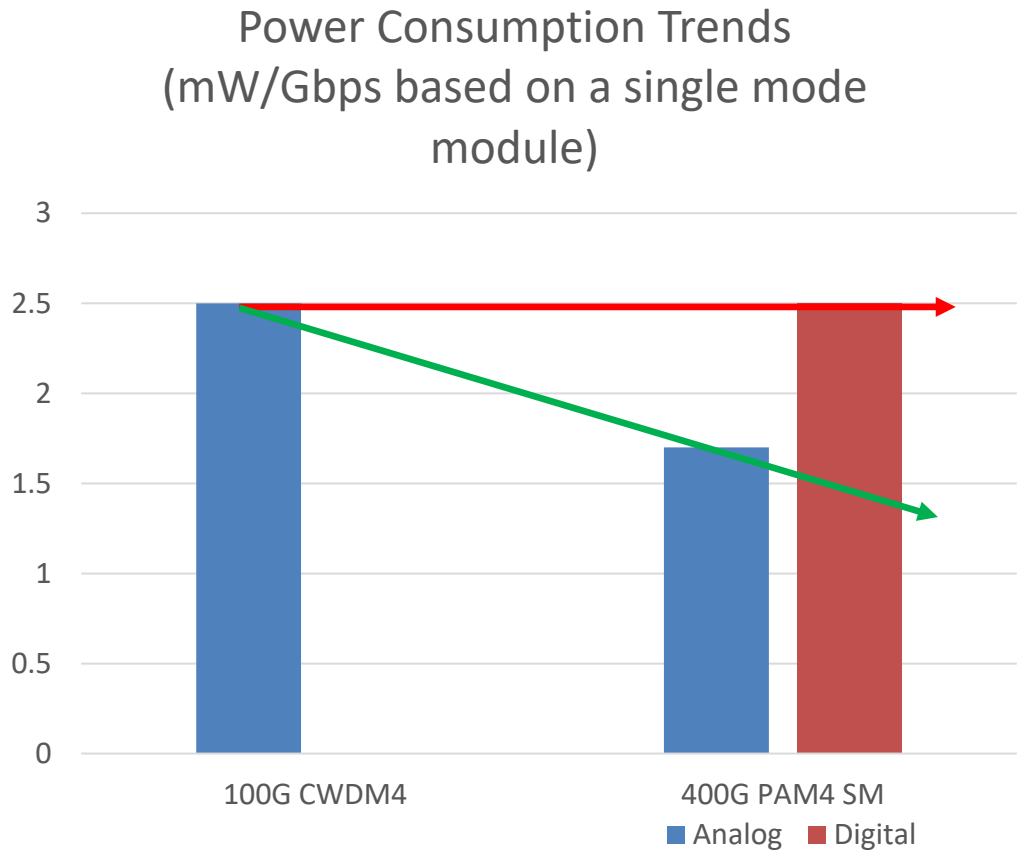
- **MSA Mission:** Simplify the industry standard optical specifications to enable utilization of multiple technologies and accelerate adoption of cost optimized 100Gbps, 200Gbps and 400Gbps optics in data center and other data communications applications
  - Phase 1: 53Gbps per lane single-mode optics
  - Phase 2: 53Gbps per lane multi-mode optics
  - Phase 3: 100Gbps per lane optics

Cost Challenges of Optics

- Cost of developing an Analog CDR in Analog Process is significantly lower than that of DSP
  - The cost of doing [5-nm] DSP is going to start approaching $80 plus million – as quoted by DSP industry
- Economics Challenge
  - Multiple device configurations are needed further driving development costs up
    - Single mode
    - Multimode
    - Single, dual, quad and octal channels (SFP, DSFP, QSFP, QSFP-DD/OSFP)
  - Total 5-years shipments of 100G modules (all reaches) 2015-2019: ~16MU
  - Amortizing $80M of DSP development cost over 16MU of parts will drive cost of modules up
  - Analog solution has both development cost and a component unit COGS advantage
- Only economics of Analog Technology can sustain needs of Optical Connectivity

Power Consumption Challenges

- **50Gbps LR1 10km module**
  - DSP based: 2.5W (2.5 mW/Gbps)
  - Analog based: <1.7W (1.7 mW/Gbps)
- **200Gbps FR4 2km module power consumption:**
  - DSP based: <5.0W (2.5 mW/Gbps)
  - Analog based <3.5W (1.7 mW/Gbps)
- **400Gbps (8x50Gbps SR8) 100m module power consumption**
  - DSP based: <10W (2.5 mW/Gbps)
  - Analog based: <7W (1.7mW/Gbps)



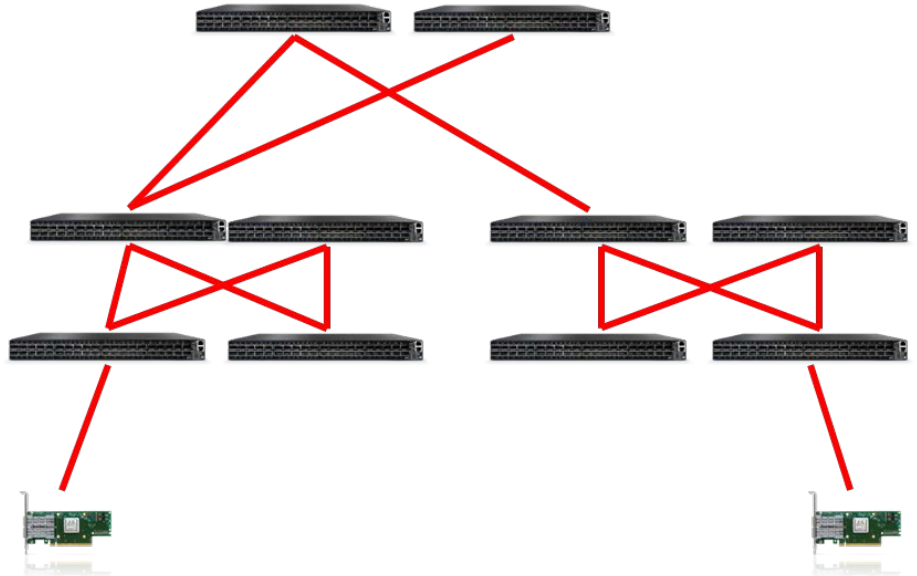
Sources: various companies' website published power numbers

Latency Implications

Cable latency multiplication

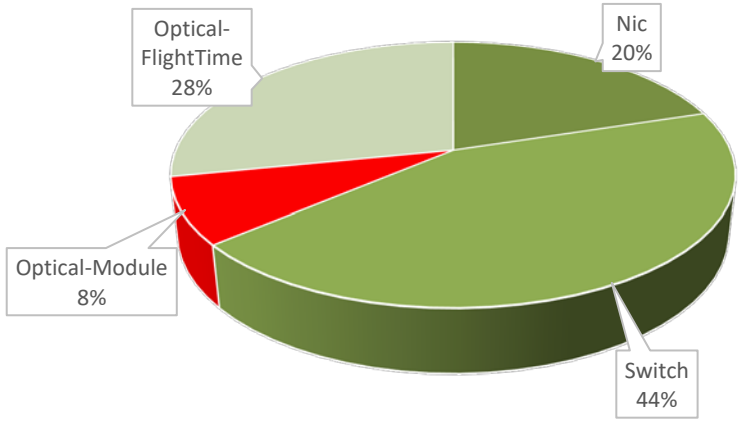
- 3-level fat tree (extract shown)
  - 6 cable hops
- Latency per unit
  - Nic 150ns
  - Switch 130ns
  - Flight time 6ns/m
  - Optical Receiver 20ns vs. 120ns

Adding ~100ns per cable for DSP is significant for HPC and AI Applications: 600ns server-to-server

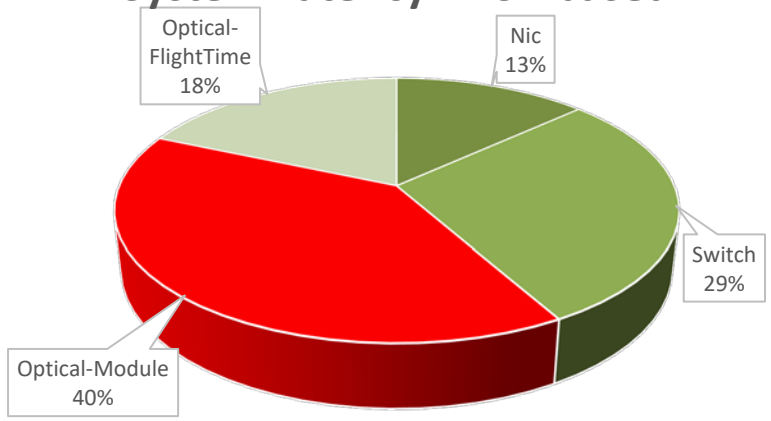


Source: Mellanox-Nvidia

System Latency – Open Eye optics



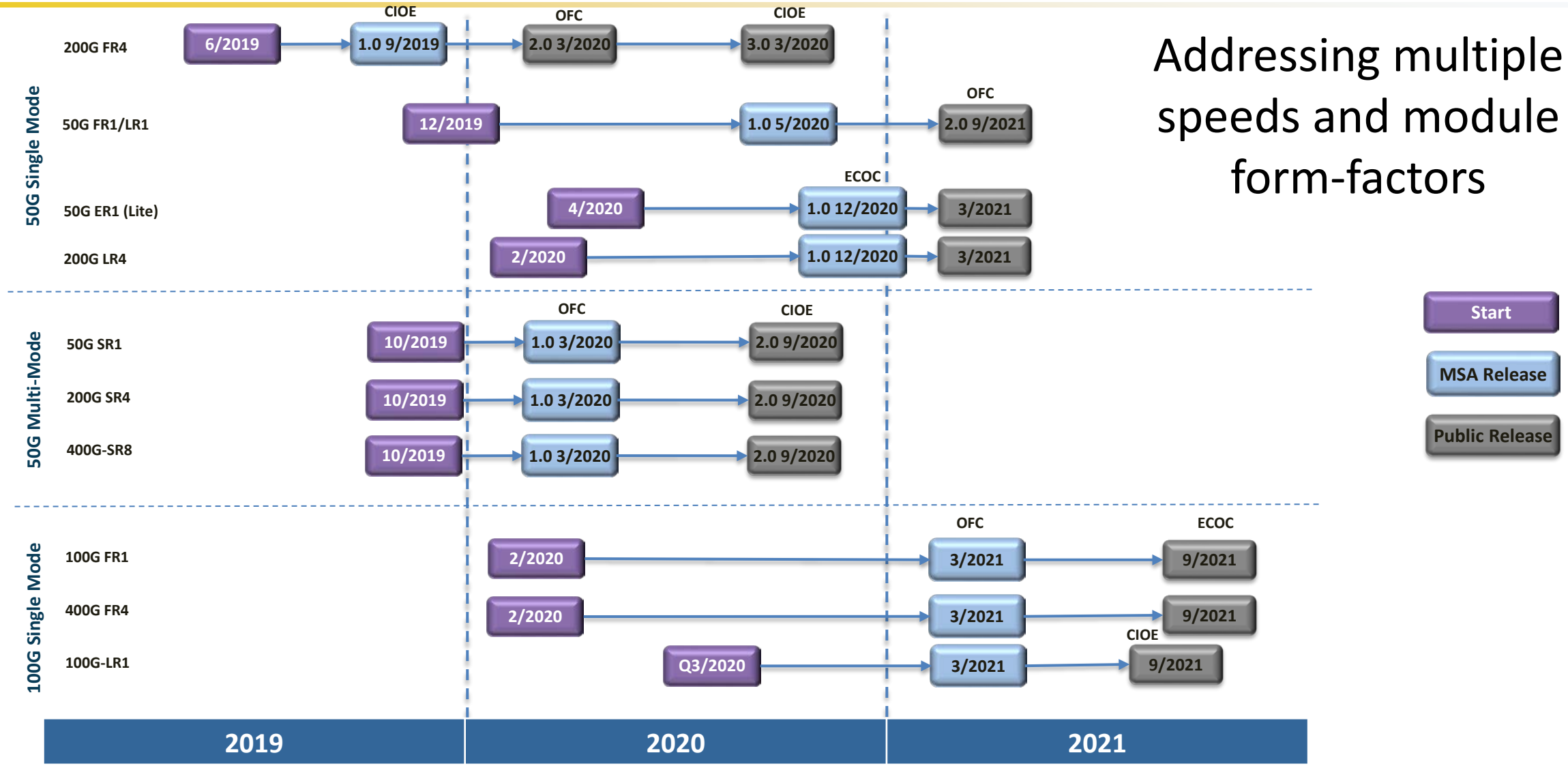
System Latency - DSP based



Open Eye MSA - Members
37 Active Members

- Established: January 2019
- Number of Founding Members: 26
- Number of Current Members: 37
- Accomplishments to Date:
  - Released 200G FR4 Single Mode Specification
  - Demonstrated multi-vendor optical interoperability
  - Demonstrated interoperability with existing 200G solutions
  - Released 50G/lane SR Multimode specification
  - Releasing soon 50G LR-1 Single Mode Specification
  - Open Eye compliant chip-level and module level products commercially available from multiple suppliers
- Parties interested in joining can contact **admin@openeye-msa.org**

Open Eye MSA - Roadmap



Addressing multiple speeds and module form-factors

Start

MSA Release

Public Release

Summary

- If you have any questions, or if you would like to join the MSA, please send an email to
  - admin@openeye-msa.org

- For more information please visit the Open Eye MSA website at: https://www.openeye-msa.org/

- Thank you for your attention